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010091789 **Image available**
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Data flow processor - uses charging logic for individual and group-wise programming of mutually orthogonal homogeneously structured cells in integrated circuit chip
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Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 4416881	A1	19941117	DE 4416881	A	19940513	199445 B
DE 4447706	A1	19970515	DE 4416881	A	19940513	199725
			DE 4447706	A	19940513	
DE 4447707	A1	19970515	DE 4416881	A	19940513	199725
			DE 4447707	A	19940513	
DE 4416881	C2	19980319	DE 4416881	A	19940513	199815

Priority Applications (No Type Date): DE 4316036 A 19930513
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4416881	A1		19	G06F-015/80	
DE 4447706	A1		1	G06F-009/38	Div ex application DE 4416881 Div ex patent DE 4416881
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DE 4416881	C2		22	G06F-015/80	Div in patent DE 4447706 Div in patent DE 4447707

Abstract (Basic): DE 4416881 A

An integrated circuit chip carries a number of mutually-orthogonal homogeneously-structured cells, each with a number of logically and structurally-identical components. The cells are combined in rows and columns, possibly also in groups, for connection to chip input/output connections.

A charging logic is associated with the cells, via which they can be programmed individually and in groups so that optional logical functions and/or networks can be verified. Manipulation of the data flow processor chip's configuration, i.e. the modification of functional parts or macros can be performed during operation without stopping other functional parts or adversely affecting their functioning.

USE/ADVANTAGE - For logical manipulation of data in binary form.

High flexibility and enables parallel operation which is scalable over wide range.

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Title Terms: DATA; FLOW; PROCESSOR; CHARGE; LOGIC; INDIVIDUAL; GROUP; WISE; PROGRAM; MUTUAL; ORTHOGONAL; HOMOGENEOUS; STRUCTURE; CELL; INTEGRATE; CIRCUIT; CHIP
Derwent Class: T01
International Patent Class (Main): G06F-009/38; G06F-015/80
File Segment: EPI

Manual Codes (EPI/S-X): T01-M05
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